REMARKS/ARGUMENTS

Enclosed herewith is a Revocation and Power of Attorney form as executed by the Assignee, including the required Statement Under 3.73(b). In that regard, during the undersigned's review of the prior attorney's prosecution file for this matter, it came to the undersigned's attention that the set of amended claims as submitted with the RCE received by the U.S. Patent Office on August 29, 2003 contained certain omissions and typographical errors as compared to the previous version of the claims, which omissions and typographical errors were not indicated as intentional amendments to the claims. As such, the listing of claims as provided in this Amendment was created on the basis that the omissions and typographical errors were, in fact, unintentional and not entered.

In the outstanding Office Action, claims 27, 29, 31 and 33 were indicated as being allowable if rewritten in independent form. Accordingly, these claims have been rewritten in independent form as new claims 35-38. The original claims 27, 29, 31 and 33 have also been retained, as it is believed that the same are allowable as depending on now allowable independent claims. Additional new claims 39 and 40 have also been added. The remaining original claims were rejected under 35 USC 102(b) or 35 USC 103 on Isaac et al. (U.S. Patent No. 4,483,726).

Claim 1 has been amended to clarify the elements of the claim by specifically setting forth that the first polysilicon layer, the interfacial oxide layer and the second polysilicon layer form a three-layer structure extending at least over the entire emitter window. Also, the limitation that the second polysilicon layer is not in direct contact with the base region has been deleted in light of the addition of the alternate claim limitation that has been made. The effect of the method of providing the three-layer structure is that upon activation of dopants in the semiconductor transistor, the interfacial oxide layer inhibits crystal growth size in the first polysilicon layer, resulting in more uniform diffusion of dopants that can increase the current gain and the speed of the transistor. In practice, the first polysilicon layer is preferably quite thin, with the interfacial oxide layer preferably being even thinner, so that crystal growth in the first polysilicon layer is limited in dimension to approximately the thickness of the first polysilicon layer. Further, the interfacial oxide layer is too thin to act as an insulator, but instead electrons easily tunnel through the very thin oxide, essentially as if the oxide was not present. Also, on activation, the interfacial oxide layer may be pierced or breached by crystal growth so that the oxide layer may not be continuous in the finished transistor. Because the interfacial oxide layer is very thin and may be broken up or discontinuous in the finished transistor, it may or may not be detectable on sectioning and inspection of the transistor, though its existence is clear by the process used for fabricating the polysilicon emitter and by the distinct difference in grain size in the first and second polysilicon layers, the transition between the small grain of the first polysilicon layer and the much larger grain size of the second polysilicon layer being clear and clearly occurring at the position of the interfacial oxide layer purposely added for that reason.

Claims 14 and 22 have been similarly amended to positively set forth the three-layer structure over the entire exposed base region. Claim 9 has been amended in a different manner, though still requiring that the first polysilicon layer cover at least the emitter window, the

interfacial oxide layer covering the first polysilicon layer within the emitter window and the second polysilicon layer covering the interfacial oxide layer within the emitter window, thereby claiming a similar structure in alternate language.

In claims 9 and 22, since the interfacial oxide layer may be broken up or discontinuous in the finished transistor, these claims have been further amended to make clear that the structure recited exists prior to annealing.

Referring now to the rejection of claim 1 and various other claims rejected under 35 USC 102(b), the Examiner compared layers 18 and 32 of Isaac et al. with the first polysilicon layer. However, clearly, polysilicon layer 32 of Isaac et al. does not extend at least over the entire emitter window, but rather is only disposed at the sides of the emitter window. Similarly, the interfacial oxide 20 and 20-1 is also only disposed at the side of the emitter window and clearly does not extend at least over the entire emitter window. While the second polysilicon layer 30 of Isaac et al. at least extends over the entire emitter window that is remaining open, it does not form the final layer of a three-layer structure formed by the method of claim 1, or for that matter, the method of claim 14 or the emitter of claim 9 or the transistor of claim 22. In that regard, Isaac et al. simply discloses an emitter 22 formed by implantation in the substrate, and thus of a monocrystalline form, in contact with base region 24, which in turn is in contact with collector region 26. The polysilicon emitter contact 30 is in direct contact with the monocrystalline emitter 22, with the polycrystalline emitter contact 30 just as well being formed by "conventional metallurgy" (column 3, starting on line 30). Accordingly, Isaac et al. simply discloses a typical monocrystalline NPN structure which may use emitter contacts of polysilicon or conventional metallurgy. Isaac et al. therefore neither discloses or renders obvious the present invention, and in fact, must be considered either not relevant to the present invention or a teaching away from the present invention.

In that regard, the inventors and the undersigned are aware that in general, transistors having polysilicon emitters are well known, not only as disclosed in the best prior art previously disclosed, but as described in other prior patents, most likely in other articles, and as practiced in prior art products. While the best known prior art has been disclosed, no representation is made that any extensive search for prior art has been made. However, as to the known prior art, such art neither discloses nor renders the present invention obvious.

For the foregoing reasons, it is believed that all independent claims in the case are now in condition for allowance, and that similarly, the dependent claims are in condition for allowance as providing greater specificity to the claims on which they depend and as adding further novel and non-obvious limitations to those combinations. In that regard, with respect to the criticality of the chosen dimensions, the thickness of the first polysilicon layer is important, because if it is too thick, it will not inhibit or restrict grain growth. Too thin is also not desirable. The thickness of the oxide layer is also important, because if it is too thick, it will restrict current flow, and if too thin, will not achieve the desired grain growth restriction.

CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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